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PATENT APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of:

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TITLE: METHOD AND APPARATUS FOR ROUTING TELECOMMUNICATIONS
 SIGNALS

Enclosed are the following papers required for a filing date under 35 CFR §1.53(b):


- ☒ Specification 16 pages
☒ Claims 11 pages
☒ Abstract 1 pages
☒ Drawings 10 sheets ☒ formal ☐ informal

The following additional papers are enclosed:

- ☐ Fee Transmittal
☐ Declaration and Power of Attorney
☐ Verified Statement(s) of Small Entity Status ☐ Independent Inventor ☐ Small Business
☐ Non-Profit ☐ Other
☐ Information Disclosure Statement ☐ Form PTO-1449
☐ Assignment and Cover Sheet
☐ Other:

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TITLE*Method and Apparatus for Routing
Telecommunications Signals*

10 This application claims the priority of Provisional Applications
60/125,527 and 60/125,533 both of which were filed on March 22,
1999. This application is also related to co-pending Application
09/274,078 which was also filed on March 22, 1999 (the same day
as the provisional applications). Applications 60/125,527,
60/125,533 and 09/274,078 are herein incorporated by reference
15 but are not admitted to be prior art.

Background of the Invention

20 Telecommunications (telecom) systems are carrying increasing
amounts of information, both in long distance networks as well as
in metropolitan and local area networks. At present, data
traffic is growing much faster than voice traffic, and includes
high bandwidth video signals. In addition to the requirement for
equipment to carry increasing amounts of telecom traffic there is
a need to bring this information from the long distance networks
25 to businesses and to locations where it can be distributed to
residences over access networks.

30 The equipment which has been developed to carry large
amounts of telecom traffic includes fiber optic transport
equipment which can carry high speed telecom traffic. The data
rates on fiber optic systems can range from millions of bits per
second (Mb/s) to billions of bits per second (Gb/s). In
addition, multiple wavelengths of light can be carried on an
optical fiber using Wavelength Division Multiplexing (WDM)
techniques.

35 The ability to carry large amounts of telecom traffic on an
optical fiber solves the long-distance point-to-point transport
problem, but does not address the issue of how to add and remove

5 traffic from the high-speed data stream. Equipment for adding and removing traffic has been developed and is referred to as "add-drop" multiplexers (ADMs).

Traditional designs for ADMs are based on the use of multiple interface cards which receive high-speed data streams, create a time division multiplex signal containing the multiple data streams, and route the time division multiplex signal to a cross-connect unit which can disassemble the data streams, remove or insert particular data streams, and send the signal to another interface card for transmission back into the networks. By aggregating the multiple data streams into a time division multiplexed data signal, the data rate of the time division multiplexed signal is by definition several times the rate of the maximum data rate supported by the interface cards. Traditional ADMs have proven adequate for interface data rates in the range of 155 Mb/s to 622 Mb/s.

However, optical signals of at least 2.4 Gb/s have become standard, and numerous problems arise with traditional ADMs due to the timing associated with the multiplexing and transmission of the high-speed signals between the interface cards and the cross-connect unit. Thus, there is a need for cross-connect equipment which can support multiple high speed data streams (i.e., at least 2.4 Gb/s).

Standardized interfaces and transmission hierarchies for telecom signals have been developed and include Pleisochronous Digital Hierarchy (PDH), Synchronous Digital Hierarchy (SDH) standards, and Synchronous Optical Network (SONET). In addition to these telecom transport standards, standards have been developed for interconnecting businesses and computers within businesses. These Metropolitan and Local Area Network (MAN/LAN) standards include Ethernet, Gigabit Ethernet, Frame Relay, and Fiber Distributed Data Interface (FDDI). Other standards, such

5 as Integrated Services Digital Network (ISDN) and Asynchronous Transfer Mode (ATM) have been developed for use at both levels.

Individual pieces of equipment can be purchased to support telecom or MAN/LAN standards. However, these devices generally either connect data streams using a signal protocol or convert
10 entire data streams from one protocol to another. Thus, there is a need for a device which can establish interconnectivity between interfaces at the MAN/LAN level, while providing cross-connection to interfaces at the telecom network level.

Multiple interfaces are presently supported in cross-connect
15 equipment using different interface cards. High-speed interface cards must be inserted into particular slots in order to insure that the high-speed signals can be transported to and from the cross-connect unit and to and from the high-speed interface cards. It would be desirable to have a cross-connect system in
20 which all cards can support high-speed optical signals of at least 2.4 Gb/s, regardless of the card slot they are located in. Moreover, it would also be useful to have a system which would support routing, bridging, and concentration functions within MANs/LANs, as well as permitting access to telecom networks.

25 For the foregoing reasons, there is a need for a flexible cross-connect apparatus that includes a data plane and can support multiple high-speed optical interfaces in any card slot. Furthermore, the flexible cross-connect apparatus should establish connectivity between data cards and the telecom
30 networks.

Summary of the Invention

The present invention discloses a method and apparatus for cross-connecting high-speed telecommunications signals at a
35 cross-connect apparatus. The cross-connect apparatus can transmit the telecommunications signals from an input interface card to a cross-connect card, and from the cross-connect card to

5 an output interface card without any synchronization information. Synchronization of the signals is accomplished with circuitry contained on the interface cards and the cross-connect card. The cross-connect apparatus also includes a control unit for managing the control and timing of the apparatus.

10 According to one embodiment, an apparatus for flexibly transmitting data from at least a first interface card to at least a second interface card is disclosed. The apparatus is capable of supporting multiple types of interface cards and includes a plurality of interface cards for transmitting and
15 receiving data streams. A cross-connect unit receives data streams from at least one of the plurality of interface cards and combines the received data streams so as to generate at least one cross-connected data stream. The at least one cross-connected data stream is transmitted to at least one of the plurality of
20 interface cards. A control unit controls the operation of the apparatus. A backplane forms parallel data buses for providing connectivity between each of the plurality of interface cards, the cross-connect unit, and the control unit. The data streams are transmitted between the plurality of interface cards and the
25 cross-connect unit over a clock recovery parallel bus without synchronization information.

According to one embodiment, an apparatus for routing data from at least a first interface card to at least a second interface card is disclosed. The apparatus is capable of
30 supporting multiple types of interface cards, and includes a plurality of clock recoverable interface cards for transmitting and receiving data streams having no synchronization information and a plurality of clocked interface cards for transmitting and receiving data streams including data and synchronization
35 information. A cross-connect unit receives data streams from at least one of said plurality of interface cards, combines the received data streams so as to generate at least one cross-

5 connected data stream, and transmits the at least one cross-
connected data stream to at least one of the plurality of
interface cards. A control unit controls the operation of the
apparatus. A backplane forms parallel data buses including clock
10 recovered parallel data buses and clocked parallel buses. The
parallel data buses provide connectivity between each of said
plurality of interface cards, said cross-connect unit, and said
control unit.

According to one embodiment, a method for flexibly
transmitting telecommunications signals from at least a first
15 interface card to at least a second interface using a cross-
connect apparatus is disclosed. The method includes receiving at
least a first telecommunications signal at a first interface
card. A first payload, which includes the at least a first
telecommunications signal, is transmitted from the first
20 interface card to a cross-connect unit. The first payload is
received at the cross-connect unit, which removes the first
telecommunications signal from first payload and inserts the
first telecommunications signal in a second payload. The second
payload, which includes at least the first telecommunications
25 signal, is transmitted from the cross-connect unit to a second
interface card. The first payload and the second payload do not
include synchronization information and are transmitted over a
clock recovered parallel data bus formed in a backplane of the
cross-connect apparatus.

30 These and other features and objects of the invention will
be more fully understood from the following detailed description
of the preferred embodiments which should be read in light of the
accompanying drawings.

35

Brief Description of the Drawings

The accompanying drawings, which are incorporated in and form a part of the specification, illustrate the embodiments of the present invention and, together with the description serve to explain the principles of the invention.

10 In the drawings:

FIG. 1 illustrates a block diagram of the flexible cross-connect system, according to one embodiment;

FIG. 2 illustrates a functional diagram of the flexible cross-connect system, according to one embodiment;

15 FIG. 3 illustrates communication channels between elements of the flexible cross-connect system, according to one embodiment;

FIGS. 4A and 4B illustrates the mechanical (rack) configuration of the flexible cross-connect system, according to one embodiment;

FIG. 5 illustrates the 311 MHz STS-192 bus format, according to one embodiment;

FIG. 6 illustrates the 311 MHz quad STS-48 bus format, according to one embodiment;

25 FIG. 7 illustrates the 311 MHz STS-48 bus format, according to one embodiment;

FIG. 8 illustrates the 155 MHz STS-48 bus format, according to one embodiment; and

FIG. 9 illustrates the 155 MHz STS-12 bus format, according to one embodiment.

Detailed Description of the Preferred Embodiments

In describing a preferred embodiment of the invention illustrated in the drawings, specific terminology will be used for the sake of clarity. However, the invention is not intended to be limited to the specific terms so selected, and it is to be understood that each specific term includes all technical

5 equivalents which operate in a similar manner to accomplish a similar purpose.

With reference to the drawings, in general, and FIGS. 1 through 9 in particular, the apparatus and method of the present invention are disclosed.

10 The present invention supports numerous telecommunications (telecom) and networking standards, including the following which are incorporated herein by reference:

- Bellcore Standard GR-253 CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic
15 Criteria, Issue 2, December 1995;
- Bellcore Standard GR-1230 CORE, SONET Bi-directional Line-Switched Ring Equipment Generic Criteria, Issue 3A, December 1996;
- Bellcore TR-NWT-000496, SONET Add-Drop Multiplex
20 Equipment (SONET ADM) Generic Criteria, Issue 3, May 1992;
- Bellcore Transport System Generic Requirements FR-440, Issue No. 98, September 1998; IEEE/ANSI 802.3 Ethernet LAN specification; and
- Networking Standards, by William Stallings,
25 published by Addison-Wesley Publishing Company (New York, 1993).

FIG. 1 illustrates a block diagram of a flexible cross-connect system 10 capable of routing traffic across two high-
30 bandwidth planes. The flexible cross-connect system 10 includes a telecom plane 100, such as a SONET plane, and a data plane 110. The telecom plane 100 includes telecom plane network interface subsystems 130, and the data plane 110 includes data plane network interface subsystems 140. A centralized fully non-
35 blocking cross-connect unit (XC) 120 is located in the telecom plane 100, which interfaces with the telecom plane network

5 interface subsystems 130 and the data plane network interface subsystems 140.

Standardized telecom traffic, such as SONET, Synchronous Digital Hierarchy (SDH) and Pleisochronous Digital Hierarchy (PDH), enters the system through the telecom plane network interface subsystems 130, such as electrical or optical interface subsystems. The telecom traffic is transmitted from the telecom plane network interface subsystems 130 over point-to-point connections 150 to the XC 120. The XC 120 processes the telecom traffic and then transmits the processed data back to a telecom network, such as a Wide Area Network (WAN), or transmits the processed data to a data network, such as a Metropolitan or Local Area Network (MAN/LAN). The processed data is transmitted to the telecom network via the telecom plane network subsystem(s) 130, and to the data network via the data plane network interface subsystem(s) 140.

Standardized telecom signals include, but are not limited to, DS-1 (1.5 Mb/s), B-ISDN (1.5Mb/s) DS-2 (6.3Mb/s), DS-3 (44.7 Mb/s), CEPT-1 (2.048 Mb/s), CEPT-2 (8.45 Mb/s), CEPT-3 (34.37 Mb/s), CEPT-4 (139.3 Mb/s), electrical STS-1 and its multiples, electrical STM-1 and its multiples, and optical OC-1 and its multiples. Other standardized and non-standardized transmission signal formats can be supported and are understood by those skilled in the art.

Standardized data traffic, such as Ethernet, enters the system through the data plane network interface subsystems 140, such as electrical or optical interface subsystems. The data plane network interface subsystems 140 communicate with the XC 120 via point-to-point connections 150. The data plane 110 also allows for communications between data plane network interface subsystems 140 via point-to-point connectors 160. Thus, the data traffic can be processed by multiple data plane interface subsystems 140 before being transmitted to the XC 120 or back to

5 the data network. As with the telecom traffic, the XC 120 processes the data traffic and transmits the processed data to a telecom network or a data network.

Standardized data signals include, but are not limited to, packet data transport formats such as Frame Relay, Asynchronous
10 Transfer Mode (ATM), and Integrated Services Digital Network (ISDN); and MAN/LAN formats such as Ethernet, Fiber Distributed Data Interface (FDDI), and Token Ring. The interfaces supported by the data plane network interface subsystems 140 include
15 electrical Ethernet interfaces such as 10BaseT and 100BaseT, as well as optical interfaces such as 1000BaseT and Gigabit Ethernet. Other data-centric interfaces can be used and are understood by those skilled in the art.

In one embodiment, the point-to-point connections 150 between the XC 120 and the telecom plane network interface
20 subsystems 130 or between the XC 120 and the data plane network interface subsystems 140 are all in a single specified format. For example, in a preferred embodiment, all the point-to-point connections 150 are high-speed connections realized as Synchronous Transfer Signal (STS)-192 formatted signals. The
25 STS-192 signals are transported on a multi-trace electrical bus formed on a high-speed backplane.

In an alternative embodiment, as illustrated in FIG. 2, specific network interface subsystems are designated as high-speed interface subsystems 200 and others are designated as low-speed interface subsystems 220 having corresponding high-speed
30 connections 230 and low-speed connections 240 to the XC 120. For example, the low-speed interconnections 240 may operate at the STS-48 rate of 2.488 Gb/s, while the high-speed interconnections 230 may operate at the STS-192 rate of 9.953 Gb/s.

35 The high speed network interface subsystems 200 may be realized as printed circuit boards containing active and passive electrical and optical components, and may contain multiple

5 network interfaces 202 operating at the same or different speeds.
The low speed network interface subsystems 220 may also be
realized as printed circuit boards with active and passive
electrical and optical components, and can contain multiple
network interfaces 202 operating at the same or different speeds.
10 As an example, a low speed network interface subsystem 220 can be
realized as a DS-1 interface board supporting 14 DS-1 interfaces.
Alternatively, a low speed network interface subsystem 220 can be
realized as an Ethernet board supporting multiple Ethernet
interfaces.

15 As illustrated in FIG. 3, the XC 120 has direct point-to-
point connections 150 with each interface subsystem 301, 302,
303, 304, 309, 311, 312, 313, 314, 319. Each of the interface
subsystems 301-304, 309, 311-314, and 319 represents an interface
card which is either of the class of cards which are telecom
20 plane network interface subsystems 130 (high-speed) or which are
data plane network interface subsystems 140 (low-speed). The
designation L and R in network interface subsystems 301-304, 309,
311-314, and 319 are used to simply designate left-hand side or
right hand-side of a mechanical configuration, but are not
25 intended to be architectural limitations.

Referring to FIG. 3, there are multiple point-to-point
System Communication Links (SCLs) 352 between a centralized
timing, control, and communications subsystem (TCC) 300 and each
of the interface subsystems 301-304, 309, 311-314, and 319. The
30 TCC 300 is also directly connected to the XC 120 via a TCC to XC
communication bus 360. In a preferred embodiment, the system has
a redundant XC 325 and a redundant TCC 305.

FIGs. 4A and 4B illustrates the system as a rack with card
slots. The rack consists of a card cage, a backplane 800, and
35 set of plug-in cards. Mechanical card guides and backplane
connectors 801 on the backplane 800 form card slots 403. As
illustrated, the card slots 403 in the card cage are numbered

5 from 1 to 17, left to right. The plug-in cards are grouped into two general groups. The first group is the common equipment cards, which include a XC card 440, a redundant XC card 442, a TCC card 430, a redundant TCC card 432, and a Miscellaneous Interface Card (MIC) 450. The second group is the network
10 interface cards and includes low speed cards 420 and high speed cards 400, which form the telecom plane network interface subsystems 130 and the data plane network interface subsystems 140.

As illustrated in FIG. 4A, high-speed network interface
15 cards 400 and low speed network interface cards 420 are supported. In one embodiment, the high speed network interface cards 400 support one or more electrical and optical interfaces up to Optical Carrier (OC)-192 data rates, while the low speed network interface cards 420 support data rates of up to OC-48.
20 Traffic carried through these network interfaces is routed over the backplane 800 to the XC card 440 or the redundant XC card 442.

The point-to-point connections 150 are realized on the backplane 800. In one embodiment, the backplane is a multi-layer
25 board that is capable of providing multiple point-to-point connections 150 between the same devices. In a preferred embodiment, the backplane is capable of transmitting different rate payloads (high-speed and low-speed). Moreover, the backplane is capable of forming data buses that can transmit
30 payloads over different rate data buses. That is, the flexible cross-connect system 10 can be designed to be backward compatible and support payload rates for currently used (or standard) cards at currently used (or standard) data bus rates. In a preferred embodiment, the data buses are formed in the backplane 800 using
35 end-terminated controlled impedance traces and the signals are transmitted between the interface cards and the XC card 440 as single-ended Gunning Transistor Logic (GTL) signals.

5 In one embodiment, the point-to-point connections 150 which support high-speed interface cards (STS-192 interface cards) and transmit STS-192 payloads, are realized as a 32-bit parallel data bus operating at 311.04 MHz. The 32-bit parallel bus transmits 32 data signals without any sync or clock signals. Clock recovery is performed at the receiving end, and will be described in more detail later. The 32-bit parallel bus is made up of four 8-bit buses. The STS-192 frame consists of 155,520 bytes. FIG. 5 illustrates the 311 MHz STS-192 bus format. As illustrated, four 8-bit buses, parallel to each other, make up the 32-bit parallel bus. The buses are labeled as carrying 8-bits of a 32-bit word, that is bits 0-7, 8-15, 16-23, and 24-31. As illustrated, the first set of bytes is the last 4 bytes of an STS-192 frame, and the second set is the first 4 bytes of the next frame. Each byte is one cycle of the 311.04 MHz recovered clock and is approximately 3.215 ns.

In an alternative embodiment, the point-to-point connections 150 which support high-speed interface cards (STS-192 interface cards) can also support a "quad-STS-48" mode, wherein each of the four 8-bit buses support an independent STS-48 frame. FIG. 6 illustrates the 311 MHz quad-STS-48 bus format. As illustrated, four 8-bit buses are each carrying a STS-48 stream, and each bus recovers its own 311.04 MHz clock.

In one embodiment, the point-to-point connections 150 which support low-speed interface cards (STS-48 interface cards) and transmit STS-48 payloads are realized as an 8-bit data bus operating at 311.04 MHz. The 8-bit bus transmits 8 data signals without any sync or clock signals. Clock recovery is performed at the receiving end, and will be described in more detail later. The STS-48 frame consists of 38,880 bytes. FIG. 7 illustrates the 311 MHz STS-48 bus format. As illustrated, an 8-bit bus is utilized to carry the STS-48 stream one byte at a time.

5 As previously mentioned, the flexible cross-connect system
10 is designed to support standard interface cards and cross
connect cards used in current cross-connect systems. These
standard interface and cross-connect cards do not support such
high-speed data rates (STS-192) and also do not perform clock
10 recovery functions. Designing the flexible cross-connect system
10 in this manner allows the standard interface and cross-connect
cards to be supported, and thus does not require that a user
update all their interface and/or cross-connect cards in order to
use the flexible cross-connect system 10.

15 In one embodiment, the point-to-point connections 150 which
support standard high-speed interface cards (STS-48 interface
cards) and transmit STS-48 payloads are realized as a 16-bit
parallel data bus operating at 155.52 MHz. The 16-bit parallel
bus transmits 16 data signals, a sync signal, and a clock signal
20 (18 signals). The clock signals are transmitted over the data bus
from a differential clock using Low Voltage Differential Signals
(LVDS). The STS-48 frame consists of 38,880 bytes. FIG. 8
illustrates the 155 MHz STS-48 bus format. As illustrated, four
4-bit buses, parallel to one another, are used to make up the 16-
25 bit parallel bus. The 16-bit parallel bus transmits 4 bytes of
the 38,880 byte STS-48 stream at one time. It takes two clock
cycles to transmit each byte, as bits 4-7 are transmitted in a
first cycle and bits 0-3 are transmitted in a second cycle. The
clock and sync signals are transmitted along with the STS-48
30 stream. Each clock cycle is approximately 6.03 ns.

In one embodiment, the point-to-point connections 150 which
support standard low-speed interface cards (STS-12 interface
cards) and transmit STS-12 payloads are realized as a 4-bit data
bus comprising operating at 155.52 MHz. The 4-bit data bus
35 transmits 4 data signals, a sync signal, and a clock signal (6
signals). The clock signals are transmitted over the data bus
from a differential clock using Low Voltage Differential Signals

5 (LVDS). The STS-12 frame consists of 9,720 bytes. FIG. 9 illustrates the 155 MHz STS-12 bus format. As illustrated, a 4-bit bus is used to transmit the 9,720 byte STS-12 stream, $\frac{1}{2}$ byte at a time.

The following table summarizes the bus/clock modes,
10 according to one embodiment of the current invention.

Bus/Clock Mode	Narrow Bus		Wide Bus	
	Number of Bits	Data Stream	Number of Bits	Data Stream
311 MHz Clock Recovered Mode	8	STS-48	32	STS-192
155 MHz Clocked Mode	4 bits data, 1 bit sync	STS-12	16 bits data, 1 bit sync	STS-48

In a preferred embodiment, the 311 MHz bus groups the data into STS-48 byte streams. The STS-192 streams are converted into
15 four frame-locked STS-48 streams and transmitted over the backplane as such. Thus, the low-speed cards support a single stream while the high-speed slots support up to four streams. Clock recovery, optional scrambling, framing and B1 error checking are performed separately for each STS-48 stream. This
20 independent clock recovery minimizes the amount of signal "de-skewing".

Clock recovery for the 311 MHz data bus is performed by the interface cards and the XC card 440. This ensures that the protection-switching selection between the two TCCs clock outputs
25 will not cause data hits in the system 10.

Clock recovery for the XC card 440 is performed for each STS-48 stream. Clock recovery is accomplished with a per-stream phase-alignment function based on a common, one per card, reference oscillator. In a preferred embodiment, the reference
30 oscillator is a 155.52 MHz VCXO which is phase locked to a 19.44 MHz timing source within the TCC 300 with a phase-detector and a low pass loop filter. Preferably, the phase detector is located

5 on the XC card 440 and the low pass loop filter is externally
located. The 155.52 MHz oscillator is multiplied by a phase lock
loop (PLL) on the XC card 440 to obtain the 311.04 MHz clock.
The 311 MHz clock is used to drive a multi-tap delay line. The
delay line output is selected to provide an optimal clock phase
10 for receiving the STS-48 backplane streams.

Clock recovery for the interface cards is performed for each
STS-48 stream. Clock recovery is accomplished with a per-stream
phase-alignment function based on a common, one per card,
reference oscillator. In a preferred embodiment, the reference
15 oscillator is a 155.52 MHz VCXO which is phase locked in a clock
recovery PLL to one of the 311 MHz STS-48 backplane streams from
the XC card 440. The interface cards use the backplane data
timing for clock recovery to prevent large transient clock phase
differences that would occur if the interface cards and the XC
20 card 440 used the TCC reference clock. The 155.52 MHz oscillator
drives a clock doubler PLL on the interface card to obtain the
311.04 MHz clock. Since clock recovery loops are vulnerable to
false locking, the recovered clock will be frequency compared to
the 19.44 MHz reference clock from the TCC 300. If a frequency
25 error is detected the, the local clock is locked to the 19.44 MHz
reference clock.

The present system can be utilized in a variety of
configurations supporting transport of data on MAN/LAN, interLATA
and interexchange networks. Because the system can establish
30 cross connections between any interface cards and can use a data
plane 140 for local switching, a wide variety of transport
configurations can be supported, including configurations in
which a virtual LAN is created in the data plane 140, and access
to the telecom plane 130 is granted for transport to other nodes.

35 Although this invention has been illustrated by reference to
specific embodiments, it will be apparent to those skilled in the
art that various changes and modifications may be made which

5 clearly fall within the scope of the invention. The invention is intended to be protected broadly within the spirit and scope of the appended claims.

What is claimed:

1. An apparatus for flexibly transmitting data from at least a first interface card to at least a second interface card, wherein the apparatus is capable of supporting multiple types of interface cards, the apparatus comprising:

a plurality of interface cards for transmitting and receiving data streams;

a cross-connect unit for receiving data streams from at least one of said plurality of interface cards, combining the received data streams so as to generate at least one cross-connected data stream, and transmitting the at least one cross-connected data stream to at least one of said plurality of interface cards;

a control unit for controlling the operation of the apparatus; and

a backplane forming parallel data buses, including a clock recovered parallel data bus, for providing connectivity between each of said plurality of interface cards, said cross-connect unit, and said control unit, wherein the data streams are transmitted between said plurality of interface cards and said cross-connect unit over the clock recovered parallel data bus without synchronization information.

5 2. The apparatus of claim 1, wherein the clock recovered parallel data bus has a first bus rate.

 3. The apparatus of claim 1, wherein the parallel data buses support at least one bus rate.

10

 4. The apparatus of claim 1, wherein the parallel data buses further includes a clocked parallel data bus.

 5. The apparatus of claim 1, further comprising:
15 a redundant cross-connect unit; and
 a redundant control unit.

 6. The apparatus of claim 1, wherein each of said plurality of interface cards is capable of transmitting and
20 receiving data streams having a plurality of different transmission protocols.

 7. The apparatus of claim 1, further comprising a housing that includes a plurality of card slots to hold said plurality of
25 interface cards, said cross-connect unit, and said control unit.

 8. The apparatus of claim 1, wherein said backplane connects each of said plurality of card slots to all other of

5 said plurality of card slots so that a first card can communicate
with a second card regardless of the location of the cards.

9. The apparatus of claim 1, wherein all of said plurality
of interface cards are a first type that can receive data streams
10 up to a first rate, and transmit data streams to said cross
connect unit at the first rate.

10. The apparatus of claim 1, wherein:

15 a first set of said plurality of interface cards are a first
type that can receive data streams up to a first rate and
transmit data streams to said cross connect unit at the first
rate, and

20 a second set of said plurality of interface cards are a
second type that can receive data streams up to a second rate and
transmit data streams to said cross connect unit at the second
rate.

11. The apparatus of claim 2, wherein the first bus rate is
approximately 311 MHz.

25

12. The apparatus of claim 1, wherein the clock recovered
parallel data bus is a 32-bit clock recovered parallel data bus.

5 13. The apparatus of claim 9, wherein said first type of interface cards are high-speed interface cards and the first rate is an STS-192 rate.

10 14. The apparatus of claim 13, wherein STS-192 data streams are transmitted over four 8-bit clock recovered data buses in parallel to each other, forming a 32-bit clock recovered parallel data bus.

15 15. The apparatus of claim 10, wherein said first type of interface cards are high speed interface cards, the first rate is an STS-192 rate, said second type of interface cards are low speed interface cards, and the second rate is an STS-48 rate.

20 16. The apparatus of claim 15, wherein STS-192 data streams are transmitted over four 8-bit clock recovered data buses in parallel to each other, forming a 32-bit clock recovered parallel data bus, and STS-48 data streams are transmitted over a single clock recovered 8-bit data bus.

25 17. The apparatus of claim 1, wherein a first set of said plurality of interface cards support a first set of interface subsystems and a second set of said plurality of interface cards support a second set of interface subsystems.

5 18. The apparatus of claim 17, wherein the first set of interface subsystems forms a telecommunications plane and the second set of interface subsystems forms a data plane.

10 19. The apparatus of claim 1, wherein each of said plurality of interface cards format the received data streams, which may have a plurality of different transmission protocols, into payloads having a single format.

15 20. The apparatus of claim 1, wherein said interface cards include an oscillator that is phase locked to one of the data streams from the cross-connect unit, said oscillator used for clock recovery.

20 21. The apparatus of claim 20, wherein said oscillator is an approximately 155 MHz oscillator.

22. The apparatus of claim 1, wherein said control unit includes a reference clock.

25 23. The apparatus of claim 22, wherein said cross-connect unit includes an oscillator that is phase locked to said reference clock, said oscillator used for clock recovery.

5 24. The apparatus of claim 23, wherein said oscillator is
an approximately 155 MHz oscillator and said reference clock is
an approximately 19 MHz reference clock.

25. The apparatus of claim 4, further comprising additional
10 interface cards, wherein additional data streams are transmitted
between said additional interface cards and said cross-connect
unit over the clocked parallel data bus, the additional data
streams including data and synchronization information.

15 26. The apparatus of claim 25, wherein the clocked parallel
data bus has a second bus rate.

20 27. The apparatus of claim 25, wherein all of said
additional interface cards are a third type that can receive data
streams up to a third rate, and transmit data streams to said
cross connect unit at the third rate.

28. The apparatus of claim 25, wherein:

25 a first set of said additional interface cards are a third
type that can receive data streams up to a third rate and
transmit data streams to said cross connect unit at the third
rate, and

 a second set of said additional interface cards are a fourth
type that can receive data streams up to a fourth rate and

5 transmit data streams to said cross connect unit at the fourth rate.

29. The apparatus of claim 26, wherein the second bus rate is approximately 155 MHz.

10

30. The apparatus of claim 25, wherein the clocked parallel data bus is a 16-bit clocked parallel data bus.

31. The apparatus of claim 27, wherein said third type of interface cards are high-speed interface cards and the third rate is an STS-48 rate.

32. The apparatus of claim 31, wherein STS-48 data streams are transmitted over four 4-bit clocked data buses in parallel to each other and forming a 16-bit clocked parallel data bus.

33. The apparatus of claim 28, wherein said third type of interface cards are high speed interface cards, the third rate is an STS-48 rate, said fourth type of interface cards are low speed interface cards, and the fourth rate is an STS-12 rate.

34. The apparatus of claim 33, wherein STS-48 data streams are transmitted over four 4-bit clocked data buses in parallel to

5 each other and forming a 16-bit clocked parallel bus, and STS-12
data streams are transmitted over a single 4-bit clocked data
bus.

35. An apparatus for routing data from at least a first
10 interface card to at least a second interface card, wherein the
apparatus is capable of supporting multiple types of interface
cards, the apparatus comprising:

a plurality of interface cards including

15 a plurality of clock recoverable interface cards for
transmitting and receiving data streams having no synchronization
information, and

a plurality of clocked interface cards for transmitting
and receiving data streams including data and synchronization
information;

20 a cross-connect unit for receiving data streams from at
least one of said plurality of interface cards, combining the
received data streams so as to generate at least one cross-
connected data stream, and transmitting the at least one cross-
connected data stream to at least one of said plurality of
25 interface cards;

a control unit for controlling the operation of the
apparatus; and

a backplane forming parallel data buses including clock
recovered parallel data buses and clocked parallel buses, said

5 parallel data buses providing connectivity between each of said plurality of interface cards, said cross-connect unit, and said control unit.

36. The apparatus of claim 35, wherein data streams to and
10 from said plurality of clocked interface cards is transmitted over the clocked parallel data buses, and data streams to and from said plurality of clock recoverable interface cards is transmitted over the clock recovered parallel data buses.

37. A method for flexibly transmitting
15 telecommunications signals from at least a first interface card to at least a second interface card using a cross-connect apparatus, the method comprising:

receiving at least a first telecommunications signal at a
20 first interface card;

transmitting a first payload, which includes the at least a first telecommunications signal, from the first interface card to a cross-connect unit;

receiving the first payload at the cross-connect unit;

25 removing the first telecommunications signal from the first payload and inserting the first telecommunications signal in a second payload; and

transmitting the second payload, which includes at least the first telecommunications signal, from the cross-connect unit to a

5 second interface card, wherein the first payload and the second payload do not include synchronization information and are transmitted over a clock recovered parallel data bus formed in a backplane of the cross-connect apparatus.

10 38. The method of claim 37, wherein the at least a first telecommunications signal received by the first interface card includes a plurality of signals having different transmission protocols.

15 39. The method of claim 38, wherein the first interface card transmits the plurality of signals having different transmission protocols to the cross-connect unit at a standard transmission protocol.

20 40. The method of claim 37, further comprising pre-aligning the at least a first telecommunications signal at the first interface card prior to said transmitting a first payload.

25 41. The method described in claim 40, wherein said pre-aligning is accomplished by adjusting a programmable offset.

42. The method of claim 37, further comprising:
aggregating the telecommunications signals received from a data plane to form an aggregated telecommunication signal, the

5 data plane being formed by connecting several interface cards together; and

transmitting a third payload, including the aggregated telecommunication signal, to the cross-connect unit.

10 43. The method of claim 42, further comprising removing the aggregated telecommunication signal from the third payload and inserting the aggregated telecommunications signal in a fourth payload.

15 44. The apparatus of claim 37, further comprising:
receiving at least a second telecommunications signal at a third interface card;

20 transmitting a third payload, which includes the at least a second telecommunications signal, from the third interface card to the cross-connect unit;

receiving the third payload at the cross-connect unit;

removing the second telecommunications signal from the third payload and inserting the second telecommunications signal in a fourth payload; and

25 transmitting the fourth payload from the cross-connect unit to a fourth interface card, wherein the third payload and the fourth payload include data and synchronization information and are transmitted over a parallel clocked data bus formed in the backplane.

[illegible]

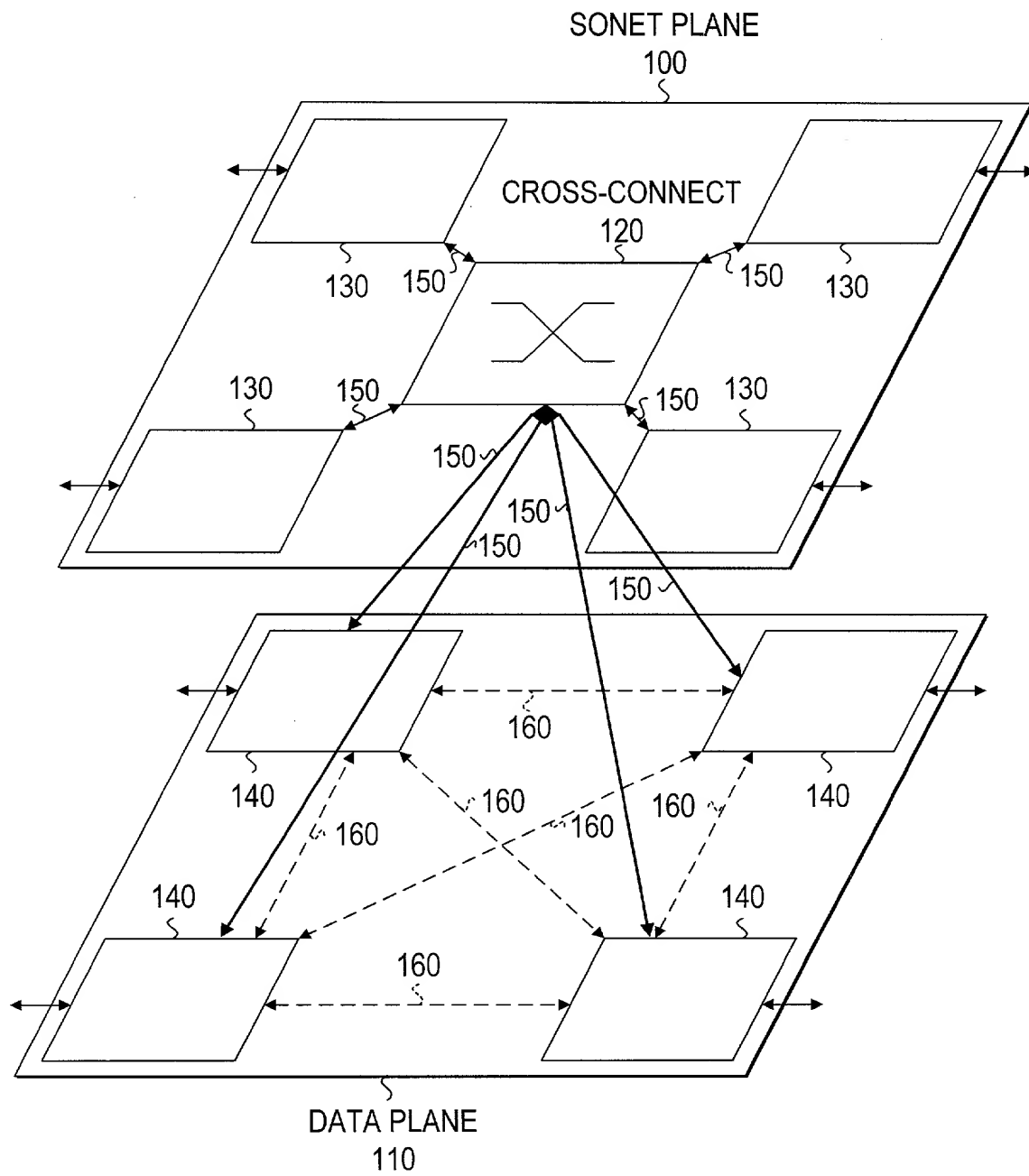


FIG. 1

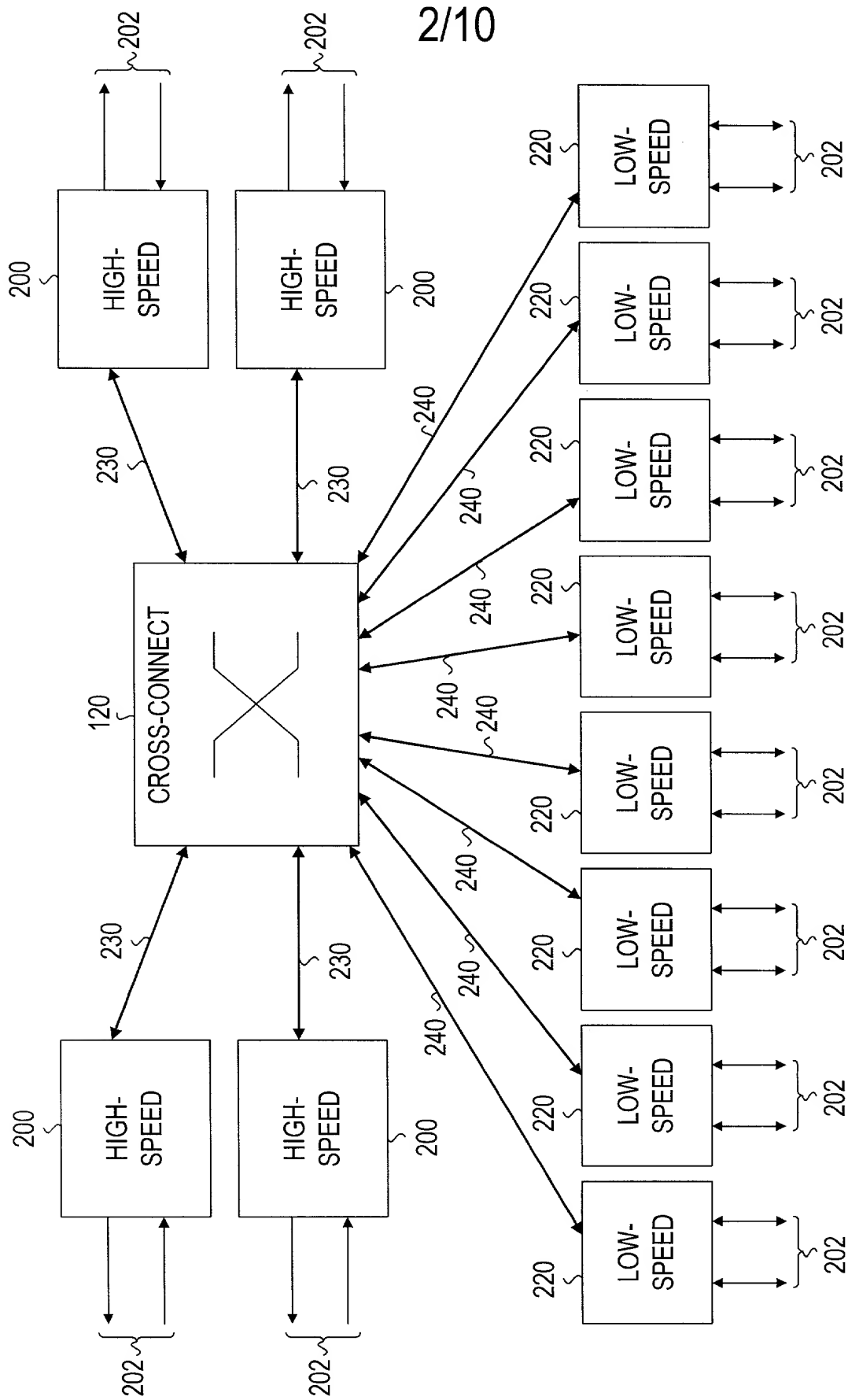


FIG. 2

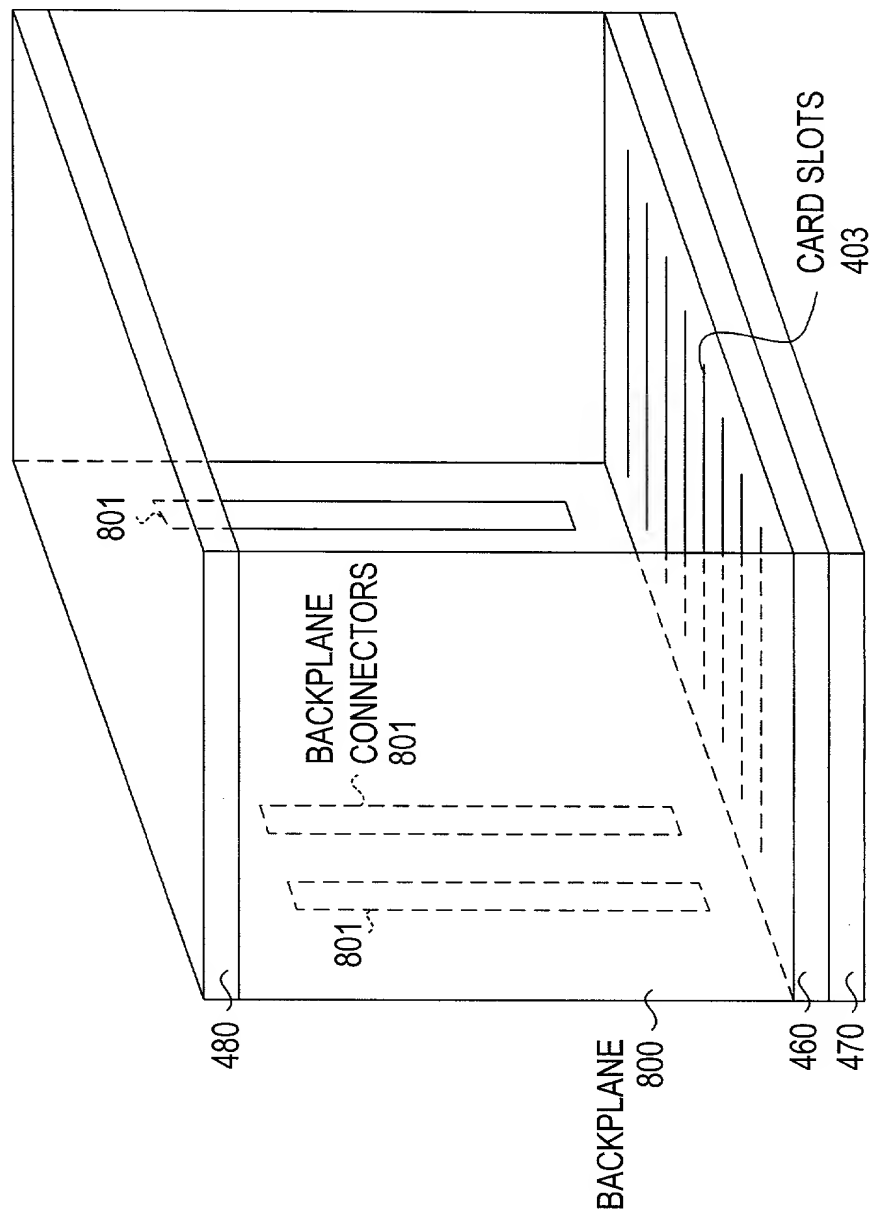


FIG. 4B

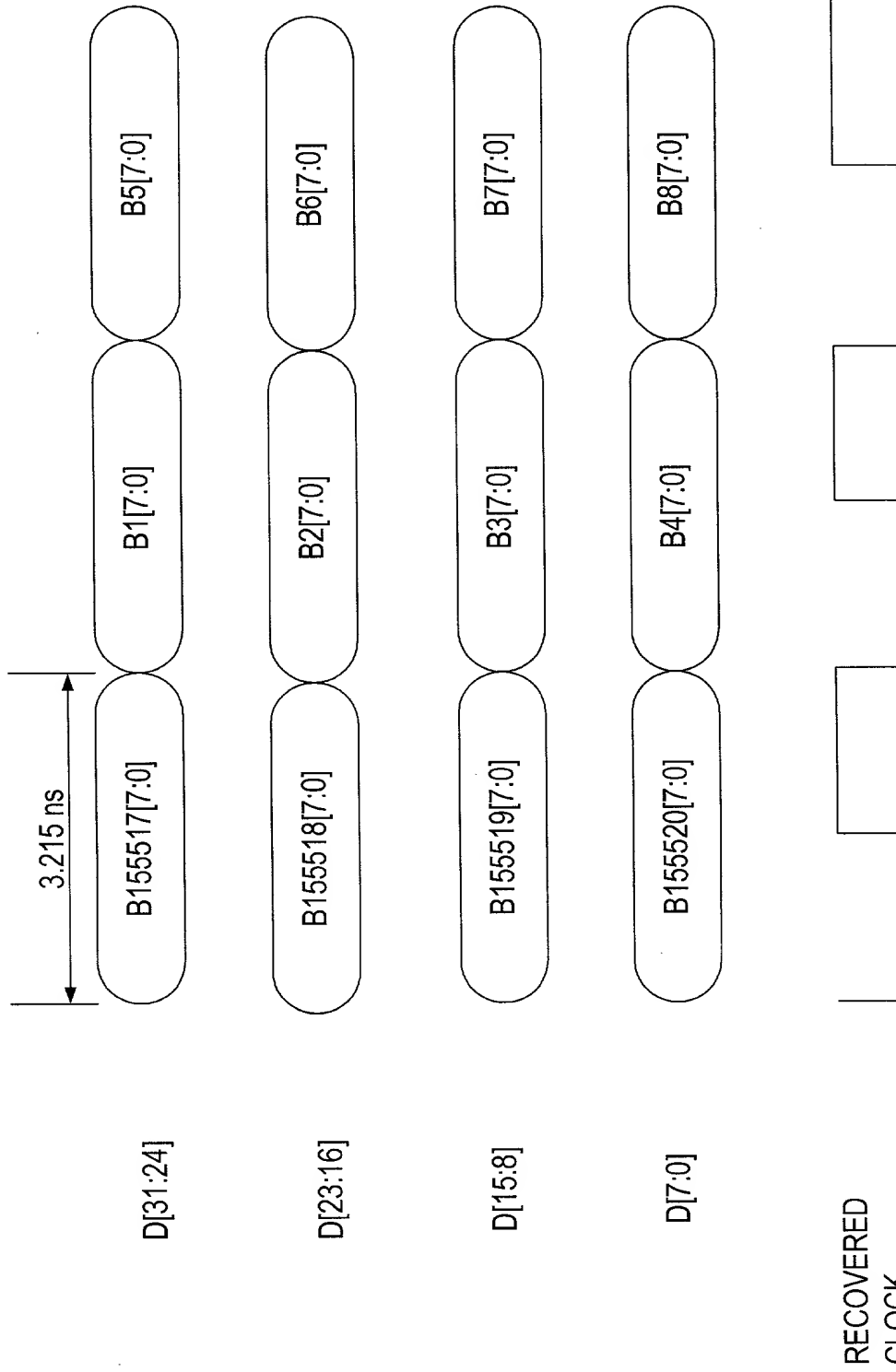


FIG. 5

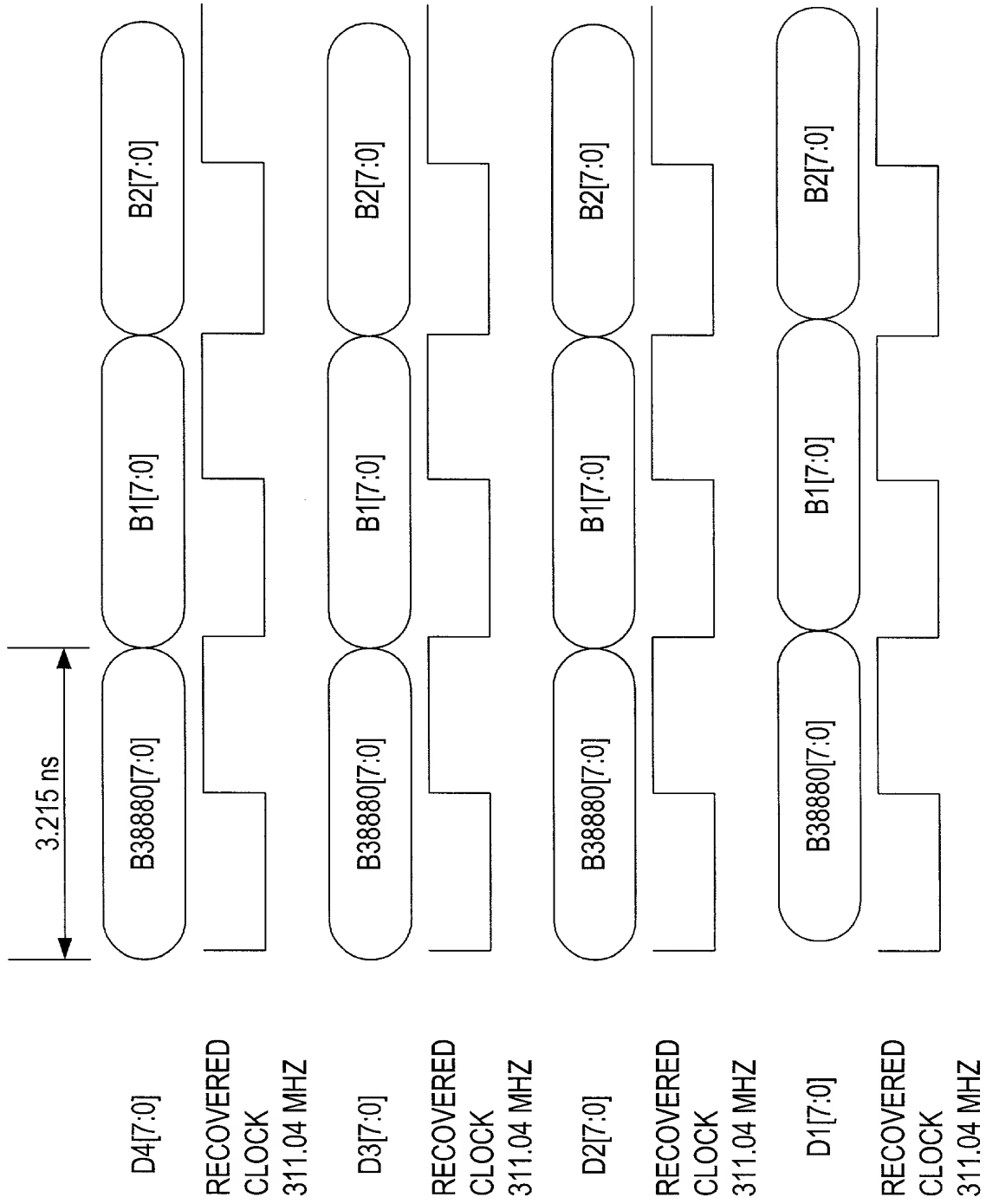


FIG. 6

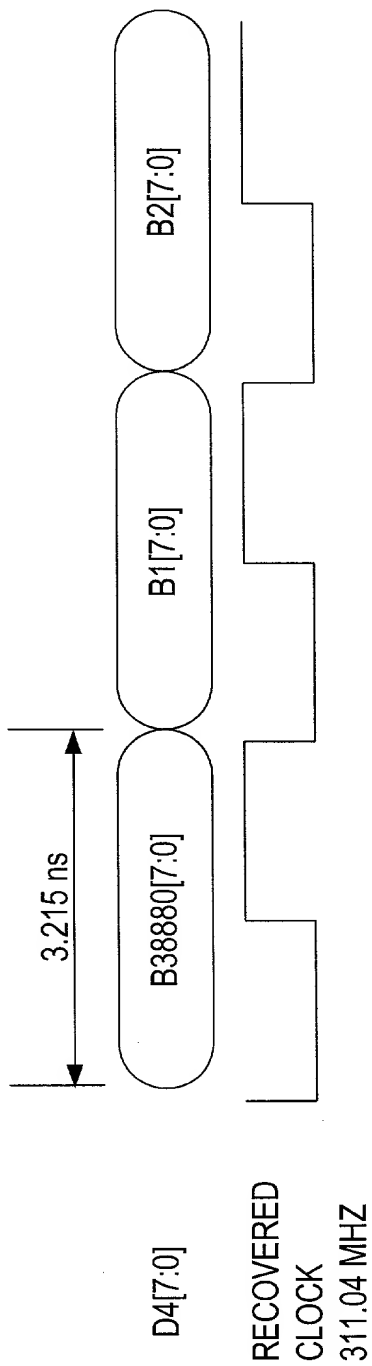
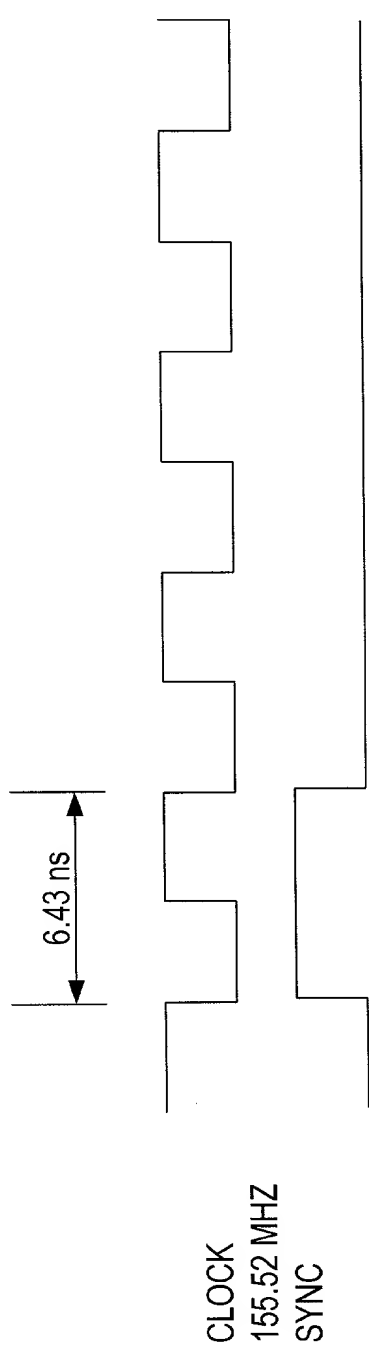


FIG. 7



D[15:12]	B38877[3:0]	B1[7:4]	B1[3:0]	B5[7:4]	B5[3:0]	B9[7:4]
D[11:8]	B38878[3:0]	B2[7:4]	B2[3:0]	B6[7:4]	B6[3:0]	B10[7:4]
D[7:4]	B38879[3:0]	B3[7:4]	B3[3:0]	B7[7:4]	B7[3:0]	B11[7:4]
D[3:0]	B38880[3:0]	B4[7:4]	B4[3:0]	B8[7:4]	B8[3:0]	B12[7:4]

FIG. 8

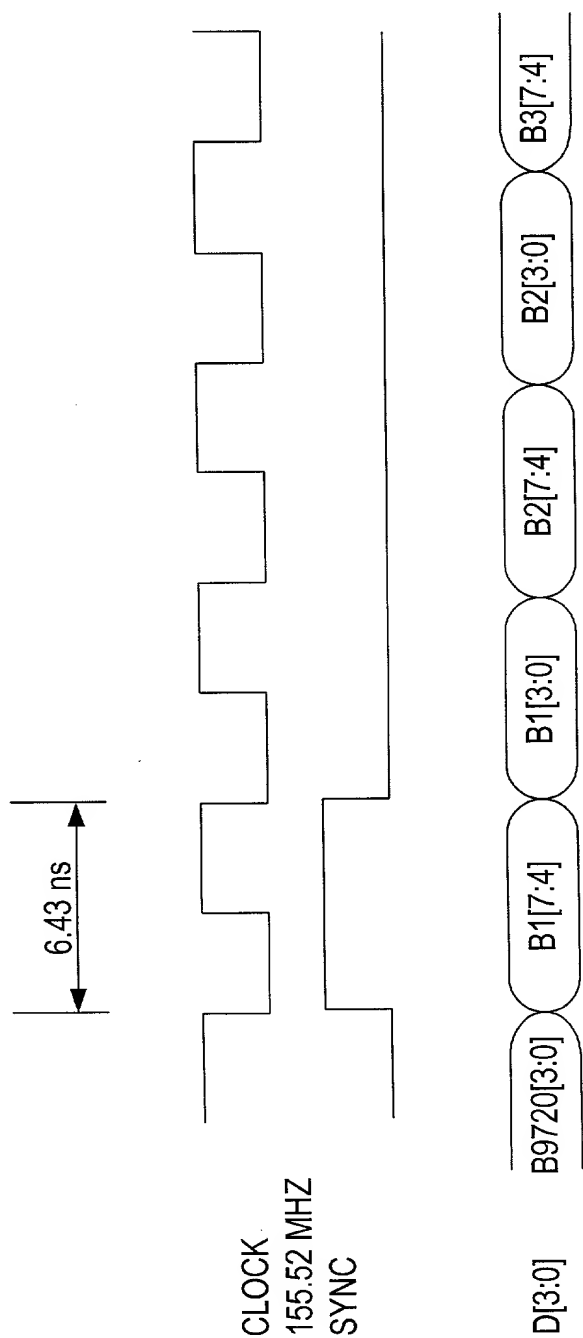


FIG. 9